and the first integer, that generates first and second estimates for each of the digital samples of the data signal; and

a linear interpolator, responsive to the first and second estimates and the second integer, that generates the interpolated digital samples;

an adaptive fractionally spaced decision feedback equalizer, responsive to the interpolated digital samples, that generates equalized digital samples at the network sampling rate in synchronization with the network clock; and

a slicer, responsive to the equalized digital samples, that generates detected symbols therefrom corresponding to data from the data signal.

3. (Amended) A receiver as recited in Claim 1, further comprising a clock synchronizer responsive to the detected symbols and generating the sampling index signal.

Please cancel Claim 5 without prejudice or disclaimer.

Please enter amended Claims 12, 14, 20 - 22, 24 - 26, and 30 as follows:

12. (Twice Amended) A method for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising the steps of:

sampling the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

generating first and second integers in response to a sampling index signal using a time converter;

interpolating the digital samples in response to the first integer to produce first and second estimates for each of the digital samples using a polyphase interpolator;

interpolating the first and second estimates in response to the second integer to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock using a linear interpolator;

equalizing the interpolated digital samples to produce equalized digital samples; and

decoding the equalized digital samples to generate detected symbols therefrom.

14. (Amended) A method as recited in Claim 12, further comprising the step of:

maintaining the synchronization between the second local sample rate and the network clock via the sampling index signal.

20. (Twice Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising:

first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

second logic configured to generate first and second integers in response to a sampling index signal using a time converter;

third logic configured to interpolate the digital samples in response to the first integer to produce first and second estimates for each of the digital samples, the third logic configured to interpolate comprising:

fourth logic configured to use a polyphase interpolator to produce the first and second estimates;

fifth logic configured to interpolate the first and second estimates in response to the second integer to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock, the second logic configured to interpolate comprising:

sixth logic configured to use a linear interpolator to produce the interpolated digital samples;

seventh logic configured to equalize the interpolated digital samples to produce equalized digital samples; and

eighth logic configured to decode the equalized digital samples to generate detected symbols therefrom.

21. (Amended) A computer program product as recited in Claim 20, wherein the seventh logic configured to equalize comprises:

ninth logic configured to use an adaptively fractionally spaced decision feedback equalizer that has tap spacing given by pT/q where T is a modulation interval associated with the network sampling rate and p and q are integers to produce the equalized digital samples.

22. (Amended) A computer program product as recited in Claim 20, further comprising:

ninth logic configured to maintain the synchronization between the second local sampling rate and the network clock via the sampling index signal.

24. (Amended) A computer program product as recited in Claim 20, wherein the receiver further includes an echo canceller coupling a transmitter to the receiver, further comprising:

ninth logic configured to receive at an input of the echo canceller transmit symbols from the transmitter that have a third local sample rate that is synchronized with the local clock; and

tenth logic configured to generate at an output of the echo canceller echo cancellation samples at the first local sample rate in synchronization with the local clock.

25. (Amended) A computer program product as recited in Claim 20, further comprising:

ninth logic configured to identify a signaling alphabet, the eighth logic configured to decode being responsive to the logic configured to identify.

26. (Amended) A computer program product as recited in Claim 25, wherein the ninth logic configured to identify comprises:

tenth logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols;

eleventh logic configured to compute an average value for the equalized digital samples corresponding to a particular alphabet threshold; and

twelfth logic configured to update the particular alphabet threshold with the average value.

30. (Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising:

first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

second logic configured to interpolate the digital samples to produce first and second estimates for each of the digital samples;

third logic configured to interpolate the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock;

fourth logic configured to equalize the interpolated digital samples to produce equalized digital samples;

fifth logic configured to decode the equalized digital samples to generate detected symbols therefrom;

sixth logic configured to identify a signaling alphabet, the fifth logic configured to decode being responsive to the logic configured to identify, the sixth logic configured to identify comprising:

seventh logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols;

eighth logic configured to compute an average value for the equalized digital samples corresponding to a particular alphabet threshold; and

ninth logic configured to update the particular alphabet threshold with the average value.